Known Issues VisualApplets Service Release 3.1

Latest Version of Known Issues Documentation

Find the latest version of our *Known Issues* documentation (containing information that might have come up after release of VisualApplets 3.1) in our live documentation:

Known Issues VisualApplets Live

Windows 10 Fall Creators update (version 1709) on a PC with a Vivado® 2017.2 or Vivado® 2017.3 Installation

If you install the Windows 10 Fall Creators update (version 1709) on a PC that has Xilinx Vivado®Registered trademark of Xilinx Corp. version 2017.2 or 2017.3 installed, Xilinx Vivado®Registered trademark of Xilinx Corp. may not properly work afterwards. Thus, you may not be able to build the designs you created with VisualApplets.

Follow the work-around provided by Xilinx Support to make your Xilinx Vivado®Registered trademark of Xilinx Corp. 2017.2 or 2017.3 installation work again. (See https://www.xilinx.com/support/answers/69908.html).

Windows 10 x64 (version 1803) Cumulative Update from 2017-07-10 (KB4338819) on a PC with a ISE®14.7 or Vivado® installation older than 2017.4

If you install the above Windows 10 update the build flow may not work properly afterwards using Xilinx tools older than Vivado® 2017.4. Thus, you may not be able to build the designs you created with VisualApplets.

For Vivado® versions older than Vivado® 2017.4 error messages may show up in the log output of the Xilinx tool chain telling that some black box instances have undefined content. For ISE® even no Xilinx tool version can be determined and the FPGA Type Check fails. Though the 32 bit tool chain of ISE® works (change the Build Settings: For *Xilinx settings batch file* use settings32.bat instead of settings64.bat).

	Follow the work-around provided by Xilinx Support to make the ISE® installation work again (See https://www.xilinx.com/support/answers/62380.html, section **ISE 14.7 64-bit - Turning off SmartHeap**). The same work-around can be used for Vivado where you need to perform the file substitution actions in the folder <VivadoInstallDir>/ids_lite/ISE/lib/nt64.

1. User-independent installation of VisualApplets in directory programs (Windows) results in access problems.
2. When you build an applet using the Xilinx Vivado Tools, you may get critical warnings (in build step LinkDesign). The warnings are due to an issue within the Xilinx tool chain. The issue is known to Xilinx and fixing is in progress. However, as this issue is NOT CRITICAL for designs created in VisualApplets, the warnings can be ignored. Example:

   > CRITICAL WARNING: [Shape Builder 18-137] Cannot obey LUTNM/HLUTNM constraint for instances …/PART1174 and …/PART1175. Illegal to place instance …/PART1174 on site SLICE_X2Y0. The location site type does not match the instance type. Instance …/PART1174 belongs to a shape with reference instance …/PART1175. Shape elements have relative placement respect to each other. The invalid location might results from a constraint on any of the instance in the shape..

3. File names: For naming *.va files, only fonts based on ASCII characters can be used; this means that, e.g., Asian, Cyrillic, Greek, or Arabic fonts are not supported for file names.
4. Bandwidth dialog in designs for microEnable 5 marathon and LightBridge frame grabbers: The values displayed for memory-based operators are not reliable. The actual data throughput of the memory operators may differ because the bandwidth analysis doesn't factor in the shared RAM concept implemented in marathon and LightBridge frame grabbers. If an operator shares the RAM with other operators, this is not detected by the bandwidth analysis and therefore is not reflected in the displayed values.
5. Only the first started instance of VisualApplets is able to save its configuration. All VisualApplets instances that have been started later have only a temporary configuration which will be discarded when the instance is closed. This concerns, e.g., build settings, library settings, system settings, general VisualApplets settings.
6. Hierarchical Boxes: If you are using hierarchical boxes, in some specific situations, the Design Rule Check may come up with the following error message: "The input XYZ of the

operator ABC (hierarchical box) must be connected to an O-type operator, e.g., NOP." The reason is that some M-type operators placed within a hierarchical box cannot be connected to the input port of the hierarchical box directly. This is only true for some specific M-type operators. You can solve this problem (within the hierarchical box) by placing an NOP operator between the input port of the hierarchical box and the input port of the M-type operator.

7. SDK for CXP: Accesses to the SISO_GenICam library are not generated automatically, but have to be programmed by the user.
8. Applets for microEnable 5 platforms have to be loaded onto the frame grabber via Firmware flasher tool (microDiagnostics) in order to change the applet.
9. Bandwidth analysis does not show exact values and is only an estimation. Please use this feature very carefully and run additional tests on the target hardware.
   Bandwidth calculation in case of kernel operations does not consider kernel dimensions.
10. Operators of the color library should be used carefully: Some color conversions don't work as a user would assume:
    - HSI2RGB converts HSL -> RGB ,
    - RGB2YUV converts RGB->YCbCr,
    - XYZ2LAB uses constants according to the following definitions: http://www.easyrgb.com/math.php?MATH=M2#text2
11. Operator *FIRKernelNxM* may cause processing errors in case parameter 'EdgeHandling' is set to constant, the number of columns > 2*parallelism, the number of kernel columns is an even number, and parallelism > 1. The error can be monitored at the left border of an image, where wrong pixel data is used at the kernel positions inside the frame.
12. Simulation of kernel images: Simulation image data cannot be fed from simulation sources into kernel positions which are unequal to (0,0).
13. After a simulation error has occurred, the simulation conditions need to be reset.
14. Trigger operators may cause spikes at the trigger output line during initialization phase when loading the applet onto the frame grabber.

15. Important note concerning operating systems Microsoft Windows 7, 8, and 10 32bit/64bit, Microsoft Windows Vista 32bit/64bit and Microsoft Windows XP 64bit:
    It is necessary and recommended to define the user folder as destination folder.
    Alternatively any other folder with full access rights can be used.
16. The DMA resource indices have to start with zero and have to be consecutively numbered. This will be checked by the DRC.
17. The operator *ImageBufferMultiRoiDyn* may cause timing errors in case of very small input images.
18. Parameters Library (VisualApplets Expert Feature): When using multiple reference operators in a chain, the references may not work correctly during runtime.
19. The operator ImageSequence may cause build errors (timing errors). (2422)
20. BAYER5x5Linear: In some cases, the resource estimation in VisualApplets for this operator (in dialog “FPGA Resource Usage”) might differ from the estimation displayed by the XilinX tools after Place & Route. (6426)

21. The dependencies of the parameters ExSyncPeriod, ExSync2Delay, and ExSyncExposure on each other are defined as follows:
    FG_LINEPERIODE >= FG_LINETRIGGERDELAY
    FG_LINEPERIODE > FG_LINEEXPOSURE
    However, at the moment it is possible to reset FG_LINEPERIODE to a value smaller than FG_LINETRIGGERDELAY and FG_LINEEXPOSURE. This may cause unexpected behaviour during runtime. (6567).

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